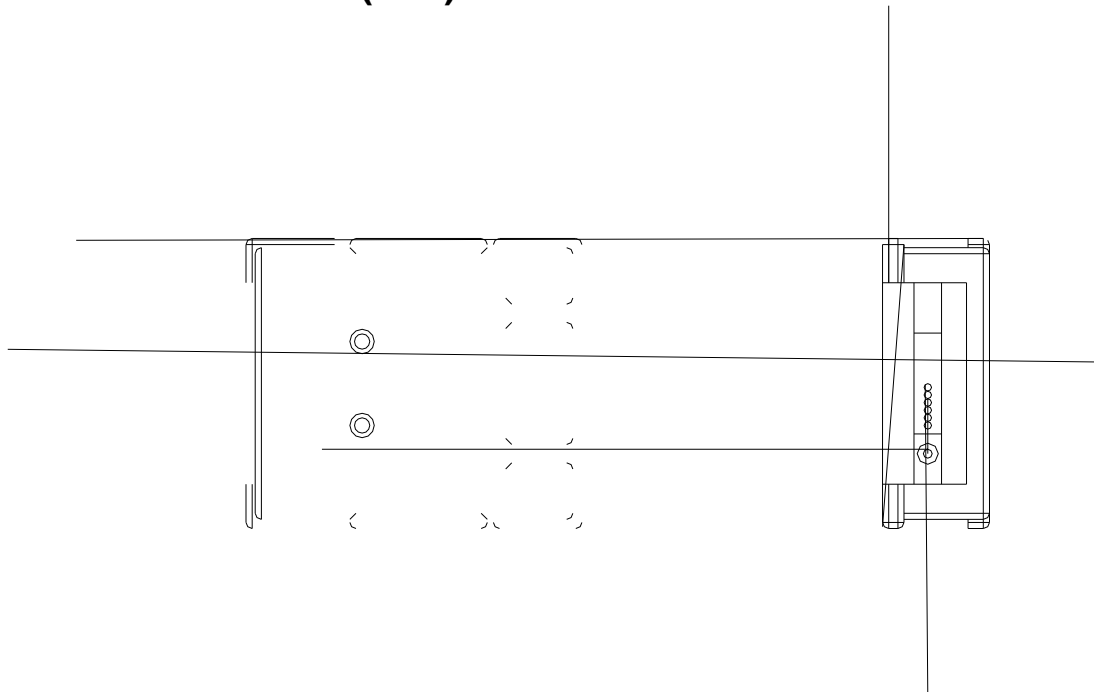


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**Receiver Optical/Electrical Characteristics**

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Damage threshold	--		3.4	--	--	dBm
Average power at receiver input, each lane		10.3125Gbps, PRBS31, BER=1*E-12 , ER=4.5dB, Output Differential Voltage = Min.290mV	-9.5	--	2.4	dBm
Optical Return Loss	ORL	--	--	--	-12	dB
Optical Modulation Amplitude (OMA), each lane	--	--	--	--	3	dBm
Peak Power, each lane	--	--	--	--	4	dBm

**Outline Dimension(mm) :**

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17	NOTINTT	<p>The active- low Interrupt (NOTINT) signal notifies the external microcontroller about driver events. These events include VCSEL operating voltage violations (VVL_x, VVH_x), input loss of signal, input signal detect and control loop faults. The polarity of the interrupt can be inverted by programming. The state of the pin may be read through the management interface.</p>
18	SDAT	<p>The Serial Data pin (SDA) is a bidirectional pin for the data signal. The pin can be tied directly to VDD of 3.3V or 2.5V. The SDA pin is I<sup>2</sup>C- bus compatible. This pad is a CMOS input/output pad. The pullup is 10 k<math>\Omega</math>.</p>
19	SCLT	<p>The Serial Clock pin (SCL) is the clock signal of the serial interface. The pin can be tied to VDD 3.3V or 2.5V. The SCL input is I<sup>2</sup>C- bus compatible and can be clocked at up to 1000kHz. The pullup is 10k<math>\Omega</math>.</p>
20	IMON	<p>The Monitor Current output (IMON) is an analog output with two functions. The IMON Select Register controls a multiplexer to select either a scaled replica of the unit current, a temperature proportional current, or, a scaled copy of the average current of a specific channel.</p> <p>By measuring the unit current during production, process dependencies are isolated and an estimate of the settings can be calculated. The average current and modulation current are derived from the unit current (<math>I_U</math>).</p> <p>The copy of the average current of an individual channel is used for real time diagnostic functions. The output is connected to ground via a resistor. A microcontroller with an integrated analog to digital converter can monitor this output and service queries from the host system.</p>



21	LDIS	<p>The Laser Disable pin (LDIS) is a global output disable signal that will set Iavg and Imod to 0 when it is high, regardless of other settings.</p> <p>The pin can be left unconnected and the device will operate normally. The state of the pin may be read through the management interface.</p>
22	VCCT	Positive supply of driver stages and VCSEL anodes
23	GNDT	Negative supply, substrate
24	GNDR	Negative supply, substrate
25		
26	VCCR	Positive supply of TIA stage and Limiting amplifier stage
27	RSSI	<p>The Receiver Signal Strength Indicator output (RSSI) pad is an analog output that sources a current proportional to the average photo-detector current on the selected channels. The output is used during manufacturing for active alignment.</p> <p>As well, the output can be configured to produce a temperature proportional output.</p>
28	NOTINTR	<p>The active- low Interrupt (NOTINT) signals notifies the microcontroller about signal detect events such as signal detect and loss of signal when the events are unmasked.</p> <p>In systems using polling-based firmware, this input may be left unconnected.</p>
29	SCLR	The Serial Clock pad (SCL) is the clock input signal of the serial interface. The pad can be tied to VDD of 3.3V or 2.5V via a resistor. The SCL input is I <sup>2</sup> C-bus compatible and operates at up to 1000kHz. If the serial interface is unused, this pad should be left unconnected.
30	SDAR	The Serial Data pad (SDA) is a bidirectional pad for the serial data signal. The pad can be tied to VDD of 3.3V or 2.5V via a resistor. The SDA pad is I <sup>2</sup> C-bus compatible and operates at up to 1000kHz. If the serial interface is unused, this pad should be left unconnected.



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31	GNDR	Negative supply, substrate
32		
33		
34		
35		
36	GNDT	Negative supply, substrate
37		
38		
39		
40		
41		

## Order Information:

### 40GBASE SR4 QSFP+ Optical Engine Preliminary

#### Statement:

SAN-U owns the authority for final explanation of all information contained in this